



2811

<b>AMENDMENT TRANSMITTAL LETTER (Large Entity)</b>			<b>Docket No.</b> BUR919990299 (01240161BA)		
Applicant(s): Adkisson et al.					
Serial No. 10/064,171	Filing Date 06/18/2002	Examiner T. Magee	Group Art Unit 2811		
Invention: <b>DOUBLE GATE TRENCH TRANSISTOR</b>					
<u>TO THE COMMISSIONER FOR PATENTS:</u>					
Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.					
<b>CLAIMS AS AMENDED</b>					
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	8 -	20 =	0 x	\$18.00	\$0.00
INDEP. CLAIMS	1 -	3 =	0 x	\$84.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT</b>					<b>\$0.00</b>
<div style="display: flex; justify-content: space-between;"><div><input checked="" type="checkbox"/> No additional fee is required for amendment. <input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of _____ <input type="checkbox"/> A check in the amount of _____ to cover the filing fee is enclosed. <input checked="" type="checkbox"/> The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 09/0456 <input checked="" type="checkbox"/> Any additional filing fees required under 37 C.F.R. 1.16. <input checked="" type="checkbox"/> Any patent application processing fees under 37 CFR 1.17.</div><div style="text-align: right;"><div style="border: 1px solid black; padding: 5px; transform: rotate(90deg); transform-origin: right top;">RECEIVED JUN - 1 2003 TECHNOLOGY CENTER 2800</div></div></div>					
<div style="text-align: center;"> Signature</div>		Dated: June 27, 2003			
<b>Marshall M. Curtis</b> Reg. No. 33,138 Whitham, Curtis & Christofferson, P.C. 11491 Sunset Hills Road, Suite 340 Reston, VA 20190 (703) 787-9400		<div style="border: 1px solid black; padding: 5px;"><p>I certify that this document and fee is being deposited on _____ with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p><div style="border: 1px solid black; padding: 5px; margin-top: 10px;"><p style="text-align: center;">Signature of Person Mailing Correspondence</p><p style="text-align: center;">Hand Delivered</p><p style="text-align: center;">Typed or Printed Name of Person Mailing Correspondence</p></div></div>			
<div style="text-align: center;"> <b>30743</b> PATENT TRADEMARK OFFICE</div>					
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of  
James W. Adkisson et al.

Serial No.: 10/064,171✓

Group Art Unit: 2811

Filed: June 18, 2002✓

Examiner: T. Magee

For: DOUBLE GATE TRENCH TRANSISTOR

Commissioner for Patents  
United States Patent and Trademark Office  
P. O. Box 1450  
Alexandria, Virginia 22313-1450

## AMENDMENT UNDER 37 C. F. R. §1.111

Sir:

In response to the Office Action mailed March 27, 2003, please amend the above-identified application as follows:

In the specification:

Please replace paragraph 0021 with the following paragraph. A marked-up copy thereof showing currently requested changes is provided in the Appendix to this response.

## Paragraph 0021:

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the  $10^{15}/\text{cm}^3$  to  $10^{17}/\text{cm}^3$  range with the high  $10^{16}/\text{cm}^3$  range being

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B<sup>1</sup>  
(contd)

preferred. The process of the present invention begins by forming a layer of pad nitride of about 100 nm thickness and a pad oxide of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

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In the claims:

Please substitute the following claim 1 for the like-numbered claim as originally filed. A marked up copy of this claim showing the current changes is attached as an appendix to this amendment.

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B<sup>2</sup>

1. (Amended) A field effect transistor comprising a conduction channel of sub-lithographic width, source and drain regions located at opposite ends of said conduction channel, said source and drain regions having silicide sidewalls on a surface thereof, and

polysilicon gate regions on opposing sides of said conduction channel and recessed from said source and drain regions, said polysilicon gate regions having silicide sidewalls formed thereon.

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REMARKS

Claims 1 - 8 remain active in this application. Claims 9-17 have previously been canceled. The specification has been reviewed and an editorial revision made where seen to be appropriate. Claim 1 has been amended to improve form. Support for the amendments of the claims is found throughout the application, particularly in Figures 4, 4A, 5 and 5A